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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,124	01/14/2002	Jimmie Earl DeWitt JR.	AUS920010714US1	2898

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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,124	DEWITT ET AL.	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/14/2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 have been examined.

2. Acknowledgement of papers filed: application and Information Disclosure Statement filed on 1/14/2002. The papers filed have been placed on record.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claims 2, 14 and 27 are objected to because of the following informalities.

5. As per claim 2, applicant states, "the registers is a dedicated-purpose register that is used to hold executed instructions." The specification (page 20) and claim 1, from which claim 2 depends, state that a copy of the executed instruction or an opcode of the executed instruction is to placed in the register. It is unclear if applicant's "executed instruction" of claim 2 is different than the previously mentioned "copy of the executed instruction" or "opcode of the executed instruction" from claim 1. Examiner will interpret the "executed instruction" of claim 2 as a "copy of the executed instruction" or "opcode of the executed instruction" as is implied by the specification and claim 1.

6. Given the similarities between claim 2 and claims 14 and 27, the arguments as stated for the objection to claim 2 also apply to claim 14 and 27.

7. Appropriate corrections are required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-8, 11-20, 23-32 and 35-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Levine et al., U.S. Patent 5,446,876, herein referred to as Levine.

10. As per claim 1, Levine teaches a method for processing an instruction within a processor, the method comprising:

-Executing an instruction within the processor: (Column 4, lines 34-39))

-And in response to completion of the executed instruction, automatically writing by the processor a copy of the executed instruction or an opcode of the executed instruction to a register within the processor: (Registers 109 and 111 contain bits that indicate if the last executed instruction was a load/store instruction or a load/store multiple instruction, the bits therefore constitute an opcode. Opcode is defined as, "A bit pattern that identifies a particular instruction." (The Authoritative Dictionary of IEEE Standards Terms, 7th Ed.))

Automatic is defined as, "acting or done as if by machine; Mechanical." (American Heritage College Dictionary, 4th Ed.) Examiner notes that a processor is an automated machine, and therefore any function a processor performs is automatically done.

11. Given the similarities between claim 1 and claims 13 and 25, the arguments as stated for the rejection of claim 1 also apply to claim 13 and 25. Examiner also notes in regards to claim 13, Levine inherently teaches means for fetching instructions from memory because it is stated that each instruction has an address in memory from which the instruction came, Column 2, lines 63-68.

12. As per claim 2, Levine teaches the method of claim 1 wherein the register is a dedicated-purpose register that is used to hold executed instructions. (Registers 109 and 111 are dedicated registers because their sole purpose is to contain bits that indicate if the last executed instruction was a load/store instruction or a load/store multiple instruction, the bits therefore constitute an opcode. (Column 7, line 63 to column 8, line 24)

13. Given the similarities between claim 2 and claims 14 and 26, the arguments as stated for the rejection of claim 2 also apply to claim 14 and 26.

14. As per claim 3, Levine teaches the method of claim 1 further comprising: determining whether or not an enable flag was previously set prior to writing the executed instruction or its opcode to a register within the processor. (Column 4, lines 47-50; there is an assertion of the trace interrupt, which is an enable flag. The trace interrupt assertion (enable flag) is checked before each instruction, therefore, on the first instruction the enable flag is checked to determine if it was previously set. For each instruction after the first instruction, the register has an executed instruction's opcode written to it. Therefore, there is a determination of the flag prior to writing the executed instruction or its opcode to a register.)

15. Given the similarities between claim 3 and claims 15 and 27, the arguments as stated for the rejection of claim 3 also apply to claim 15 and 27.

16. As per claim 4, Levine teaches the method of claim 1 further comprising: determining whether or not an interrupt-enable flag is set prior to writing the executed instruction or its opcode to a register within the processor. (Column 4, lines 47-50; there is an assertion of the trace interrupt, which is an interrupt-enable flag. The trace interrupt assertion (interrupt-enable flag) is checked before each instruction, therefore, on the first instruction the interrupt-enable flag is checked to determine if it was previously set. For each instruction after the first instruction, the register has an executed instruction's opcode written to it. Therefore, there is a determination of the flag prior to writing the executed instruction or its opcode to a register.)

17. Given the similarities between claim 4 and claims 16 and 28, the arguments as stated for the rejection of claim 4 also apply to claim 16 and 28.

18. As per claim 5, Levine teaches the method of claim 1 wherein the register is one of a plurality of registers that are used to hold executed instructions or their opcodes. (The Trace Buffer also stores an opcode value, it stores the number of bytes moved in the load/store operation, therefore the bits indicate that it was a load/store multiple instruction. (Column 9, lines 24-32 and Column 10, lines 10-45) Register is defined as, "A part of the central processing unit used as a storage location." (The American Heritage College Dictionary) The buffer entry is storing data and is in a CPU, therefore it is a register, and therefore there is a plurality of registers storing executed instruction's opcodes.

19. Given the similarities between claim 5 and claims 17 and 29, the arguments as stated for the rejection of claim 5 also apply to claim 17 and 29.

20. As per claim 6, Levine teaches the method of claim 1 further comprising:. determining whether or not a taken-branch flag is set prior to writing the executed instruction or its opcode to a register within the processor. (Column 4, lines 47-50; there is a determination of whether or not a branch was taken using the contents of a memory location, the contents of the memory location are a taken-branch flag. (Column 4, lines 51-68) The contents (taken-branch flag) are checked before each instruction, therefore, on the first instruction the taken-branch flag is checked to determine if it was previously set. For each instruction after the first instruction, the register has an executed instruction's opcode written to it. Therefore, there is a determination of the flag prior to writing the executed instruction or its opcode to a register.)

21. Given the similarities between claim 6 and claims 18 and 30, the arguments as stated for the rejection of claim 6 also apply to claim 18 and 30.

22. As per claim 7, Levine teaches the method of claim 1 further comprising: reading the register by tracing software to obtain a copy of the executed instruction or its opcode and writing the copy of the executed instruction or its opcode to persistent storage. (Column 2, line 63 to column 3, line 5 and column 8, lines 44-59)

23. Given the similarities between claim 7 and claims 19 and 31, the arguments as stated for the rejection of claim 7 also apply to claim 19 and 31.

24. As per claim 8, Levine teaches a method for processing an instruction within a processor, the method comprising:

-Executing an instruction within the processor: (Column 4, lines 34-39))

-And in response to completion of the executed instruction, automatically writing by the processor a copy of the executed instruction or an opcode of the executed instruction to a memory buffer. (Column 2, line 63 to column 3, line 5 and column 8, lines 44-59, Column 10, lines 10-45, Figure 2 and figures 3A-3D; The Trace Buffer stores an opcode value, it stores the number of bytes moved in the load/store operation, therefore the bits indicate that it was a load/store multiple instruction. Opcode is defined as, "A bit pattern that identifies a particular instruction." (The Authoritative Dictionary of IEEE Standards Terms, 7th Ed.))

Automatic is defined as, "acting or done as if by machine; Mechanical." (American Heritage College Dictionary, 4th Ed.) Examiner notes that a processor is an automated machine, and therefore any function a processor performs is automatically done.

25. Given the similarities between claim 8 and claims 20 and 32, the arguments as stated for the rejection of claim 8 also apply to claim 20 and 32. Examiner also notes in regards to claim 20, Levine inherently teaches means for fetching instructions from memory because it is stated that each instruction has an address in memory from which the instruction came, Column 2, lines 63-68.

26. As per claim 11, Levine teaches the method of claim 8 further comprising: determining whether or not a taken-branch flag is set prior to writing the executed instruction or its opcode to the buffer in memory. (Column 4, lines 47-50; there is a determination of whether or not a branch was taken using the contents of a memory

location, the contents of the memory location are a taken-branch flag. (Column 4, lines 51-68) The contents (taken-branch flag) are checked before each instruction is executed (Steps 3 and 4) to determine if the previous instruction was a branch that was taken. The opcode of the instruction is stored in the trace buffer in steps 11 & 12, a later point in time. (Figures 3A-3D)

27. Given the similarities between claim 11 and claims 23 and 35, the arguments as stated for the rejection of claim 11 also apply to claim 23 and 35.

28. As per claim 12, Levine teaches the method of claim 8 further comprising: reading the memory buffer by tracing software to obtain copies of executed instructions or their opcodes; and writing the copies of executed instructions or their opcodes to persistent storage (Disk). (Column 8, lines 44-58, the user inherently uses software to use the I/O to transmit the trace buffer data (including opcodes) to disk. Since the inherent software is transmitting trace data, it is trace software.)

29. Given the similarities between claim 12 and claims 24 and 36, the arguments as stated for the rejection of claim 12 also apply to claim 24 and 36.

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claims 9, 10, 21, 22, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine et al., U.S. Patent 5,446,876, herein referred to as Levine, in view of Gum et al., U.S. Patent 4,598,364, herein referred to as Gum.

32. As per claim 9, Levine teaches the method of claim 8 further comprising: writing variable length data to the trace memory buffer (Column 10, lines 10-45, depending on the instruction, different data is written), but is silent on how the buffer is addressed to store data in it or read data from it or if the variable length data is stored in fixed length entries. Multiple entries are written to the trace buffer in a test, as indicated by a LOC count in the profile data (Column 3, lines 41-59) and subsequently read out. It therefore is inherent that there is some method of accessing/addressing the entries in the trace buffer of Levine.

33. Since Levine is silent on the addressing of the trace buffer, for reads and writes, and the size of the entries written, Levine also fails to teach reading a register within the processor to obtain a pointer to the memory buffer.

34. Gum teaches a register (CR 12) for a tracing method that stores a next entry value (pointer) for the trace buffer. The processor reads the CR 12 register, which allows the processor to know where the next value should be written to in the trace buffer (CPU Trace Table, figure 1). This is especially useful since the tracing method of Gum includes writing variable length entries. Gum also teaches that variable length entries are beneficial because they avoid wasting space. (Column 5, lines 25-33 and lines 44-50 and Figure 6, boxes 139 and 140)

35. It would have been obvious to one of ordinary skill in the art to add the reading of the CR 12 address register of Gum to address the trace buffer in the method of Levine in order to allow variable length entries in the trace buffer, thus allowing efficient use of memory storage in the trace buffer of Levine, which produces variable length data for trace buffer storage.

36. Given the similarities between claim 9 and claims 21 and 33, the arguments as stated for the rejection of claim 9 also apply to claim 21 and 33.

37. As per claim 10, Levine teaches the method of claim 8 further comprising writing variable length data to the trace memory buffer (Column 10, lines 10-45, depending on the instruction, different data is written), but is silent on how the buffer is addressed to store data in it or read data from it or if the variable length data is stored in fixed length entries. Multiple entries are written to the trace buffer in a test, as indicated by a LOC count in the profile data (Column 3, lines 41-59) and subsequently read out. It therefore is inherent that there is some method of accessing/addressing the entries in the trace buffer of Levine.

38. Since Levine is silent on the addressing of the trace buffer, for reads and writes, and the size of the entries written, Levine also fails to teach writing a memory address for the memory buffer to a register within the processor.

39. Gum teaches a register (CR 12) for a tracing method that stores a next entry value (pointer) for the trace buffer. The processor write to the CR 12 register, then later reads the value, which allows the processor to know where the next value should be written to in the trace buffer (CPU Trace Table, figure 1). This is especially useful since

the tracing method of Gum includes writing variable length entries. Gum also teaches that variable length entries are beneficial because they avoid wasting space. (Column 5, lines 25-33 and lines 44-50 and Figure 6, boxes 139 and 140)

40. It would have been obvious to one of ordinary skill in the art to add the writing of the CR 12 address register of Gum, so as to subsequently read the register and then to address the trace buffer, to the method of Levine in order to allow variable length entries in the trace buffer, thus allowing efficient use of memory storage in the trace buffer of Levine, which produces variable length data for trace buffer storage.

41. Given the similarities between claim 10 and claims 22 and 34, the arguments as stated for the rejection of claim 10 also apply to claim 22 and 34.

Conclusion

42. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Roy et al., U.S. Patent 6,321,331, teaches a history buffer, register, enable bit and reading out data in buffer to another memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KPR

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